VLSI Question Set 1: Arijit Banerjee

1) How would you implement an inverter with a nand/ nor gate?
2) How do you implement a the equation Y=(!(!A+!B))*(!(!C+!D)) using nand gates only, nor gates only?
3) What equation we do use to simplify the Karnaugh Map?
4) What kind of code is used to simplify the K-Map?
5) For an equal sized nand and nor gates which would have larger area, and why?
6) Which of the gates have better drive strength for driving a load, nand/nor?
7) Size a nand2, nor2 gate so that it can drive 0.5fF load in 200ps for worst case condition.
8) Design a D-FF and show the setup and hold path. What is the formula for setup and hold time in this case?
9) Design a positive level trigger latch with a multiplexer of your choice. Why do you think the output of your latch will stay stable?
10) Design a decade counter with D-FFs. Design a Mod-5 counter and grey counter with J-K FF.
11) Design a detector for “10011” patterns in a serial bit stream signal.
12) Why type of substrate is usually used for bulk CMOS for fabrication, and why?
13) What is VT of a MOSFET and if I increase the doping in the channel what would happen to VT for PMOS and NMOS?
14) What are the usual best and worst case corner for leakage?
15) What are the usual best and worst case corner for delay?
16) What would happen to VT and leakage and why, if you increase temperature?
17) What are the leakage components in a MOSFET?
18) Which leakage component is the most dominating in a NMOS, PMOS?
19) Why do we need high-K gate dielectric?
20) What do we mean by dielectric coefficient?
21) Why is gate leakage increasing with device scaling and what should be done in order to minimize the same?
22) What is body bias in MOSFETs?
23) How do you get benefits out of body bias?
24) Draw and explain the I-V characteristics of an NMOS.
25) Why do we have a saturation and voltage saturation region in short channel device and not in long channel device?
26) Why do we have a subthreshold conduction in MOSFETs?
27) Why do the MOSFET subthreshold slope is 60mV/decade?
28) What do you mean by subthreshold slope is 60mV/decade?
29) What is Elmore delay and compute the Elmore delay of a nand2 gate with some assumptions.
30) What is clock feed-through? And how do you minimize the same?
31) Design a charge-pump with a capacitor and some digital gates of your choice. Why do you think the output voltage is greater than the supply voltage in your charge pump?
32) What is a 6T SRAM bitcell? Why do we need a 6T SRAM bitcell? Describe read0/write1 operation in a 6T SRAM bitcell.
33) What are the key differences between SRAM bitcell and a latch?
34) What are the failure mechanism for write and read operation for 6T SRAMs?